

PG180-A02

256b GDDR6 x16
TALL DP + DP + DP + HDMI/DP + USB

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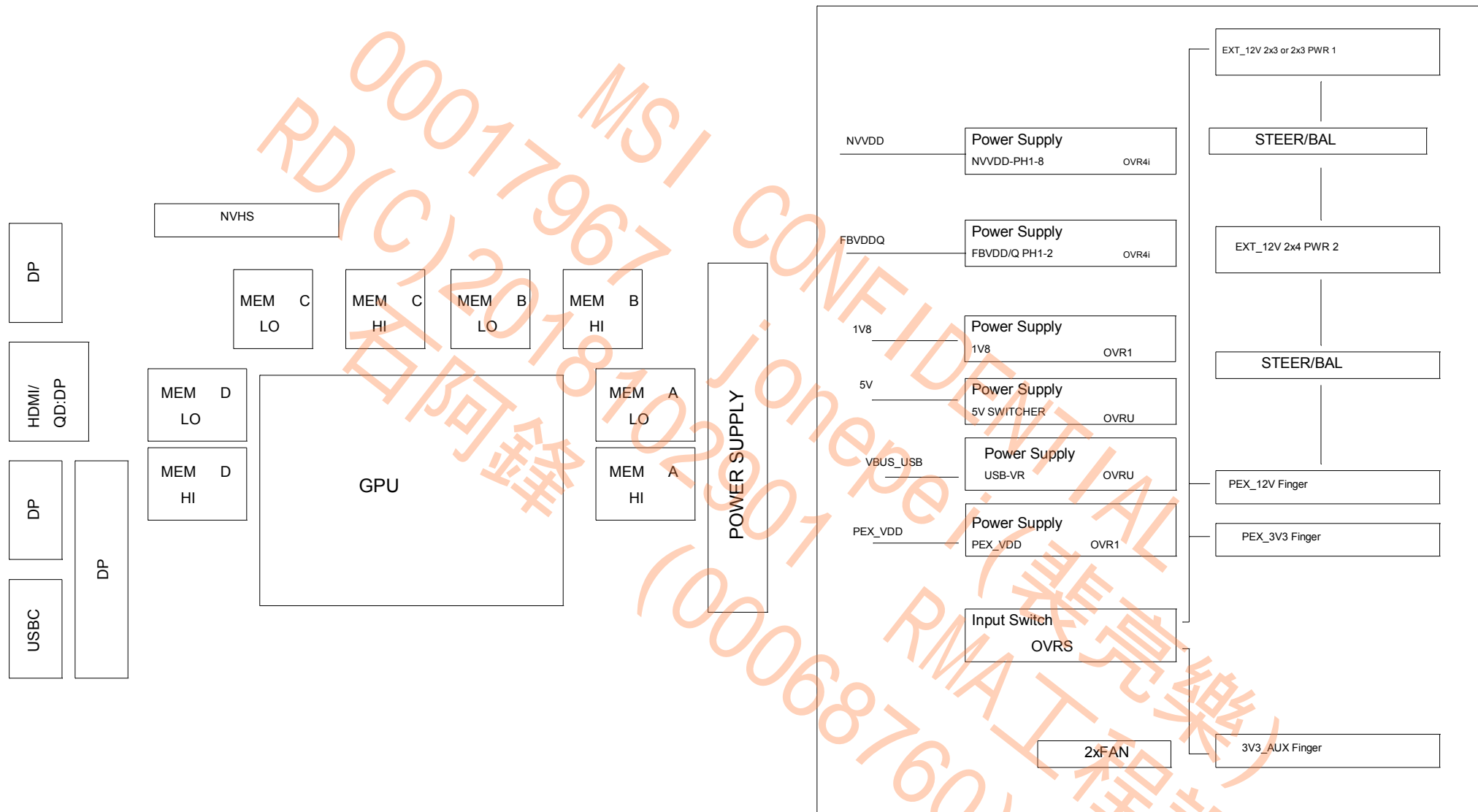
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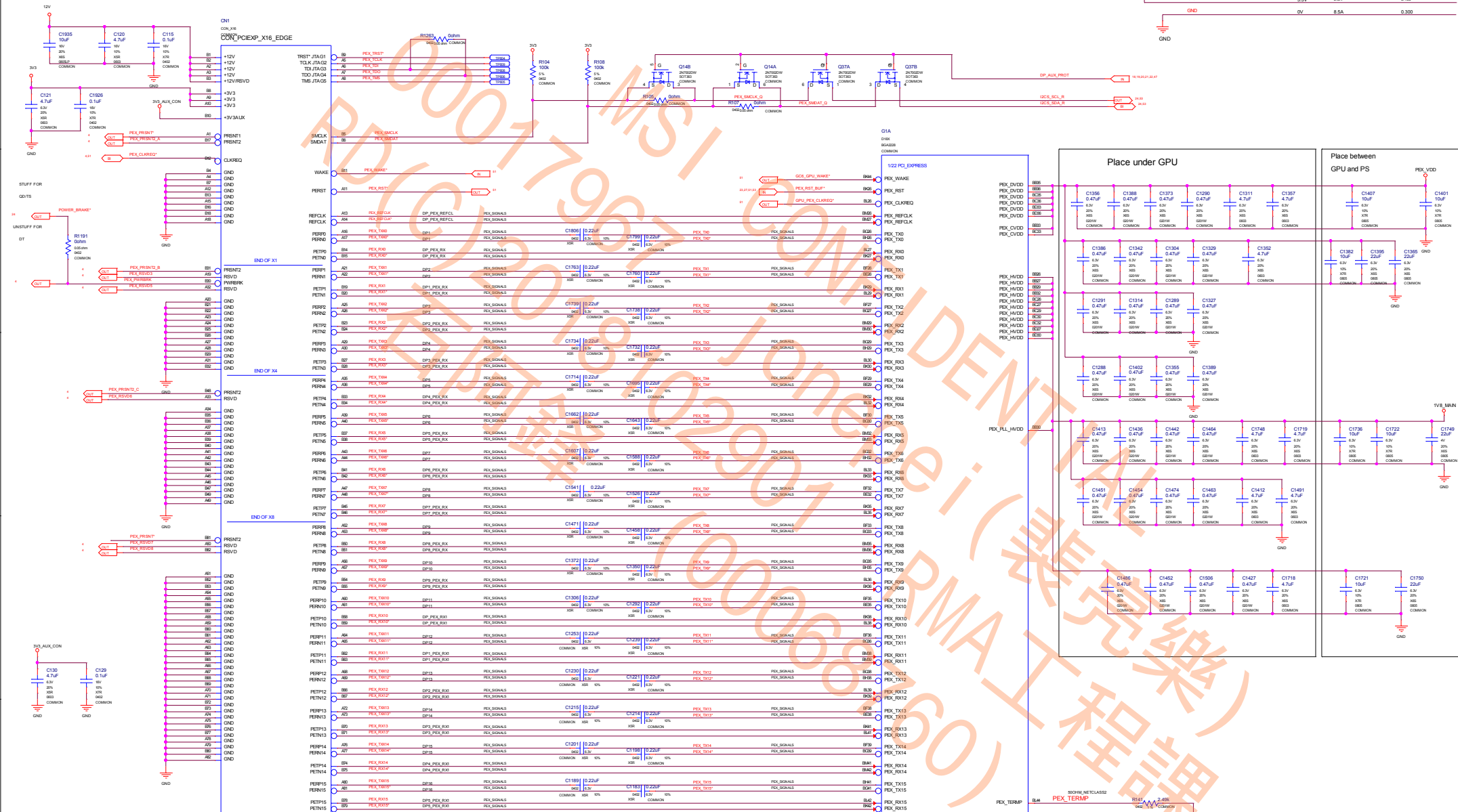




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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	Block Diagram

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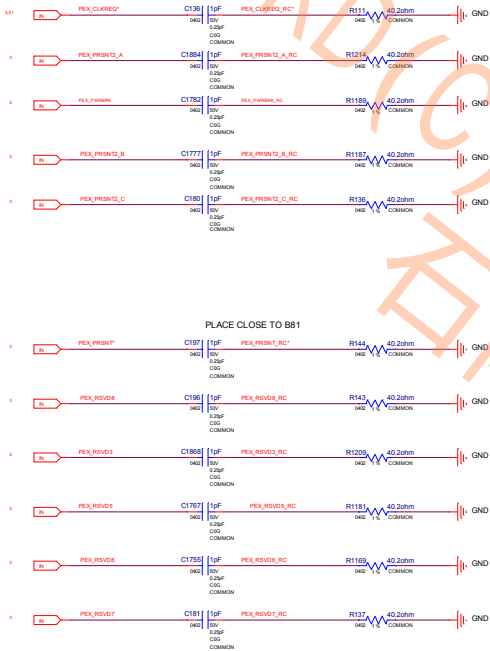
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PCB DETAIL	PCI Express



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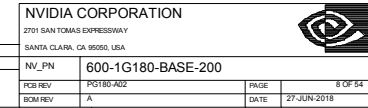
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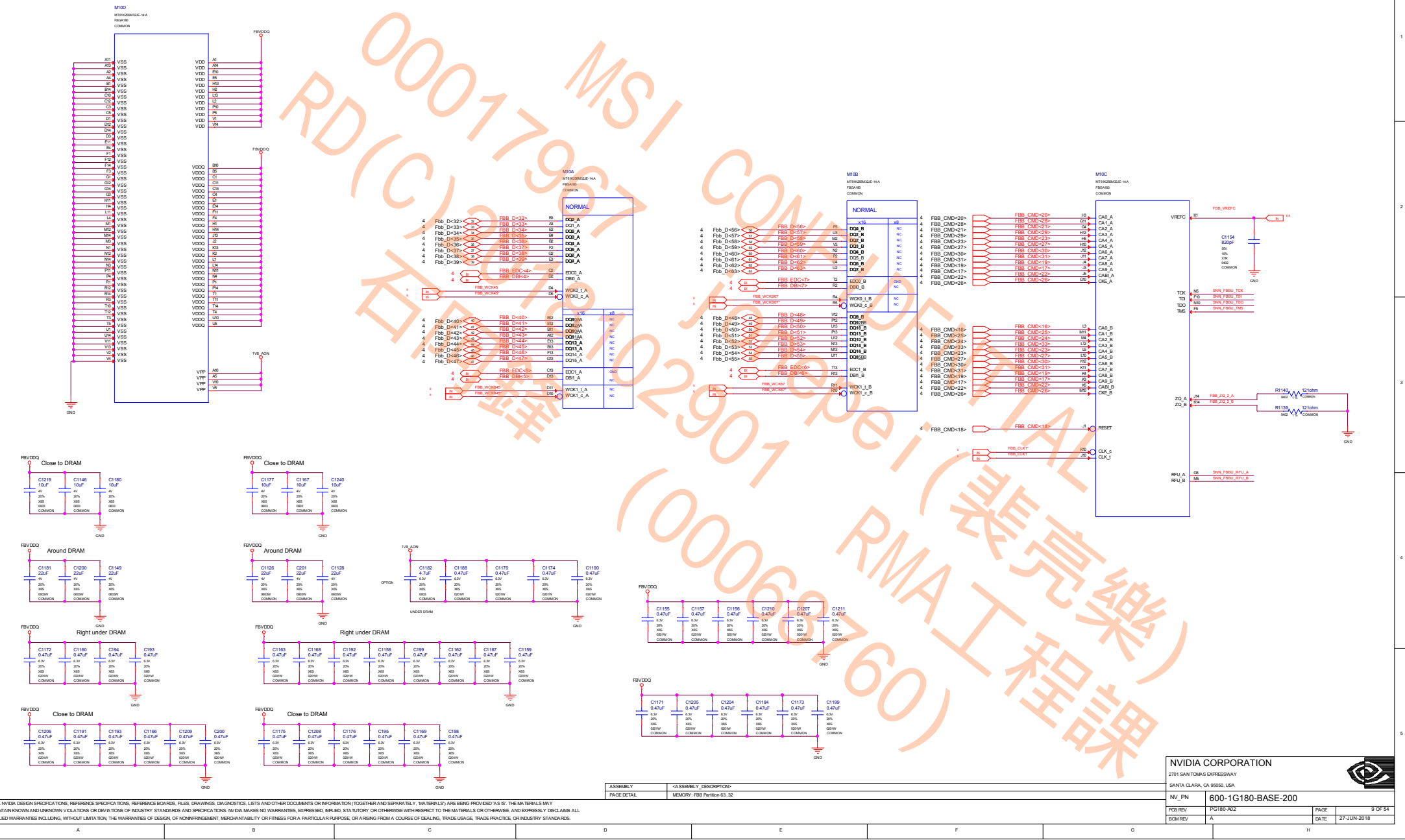


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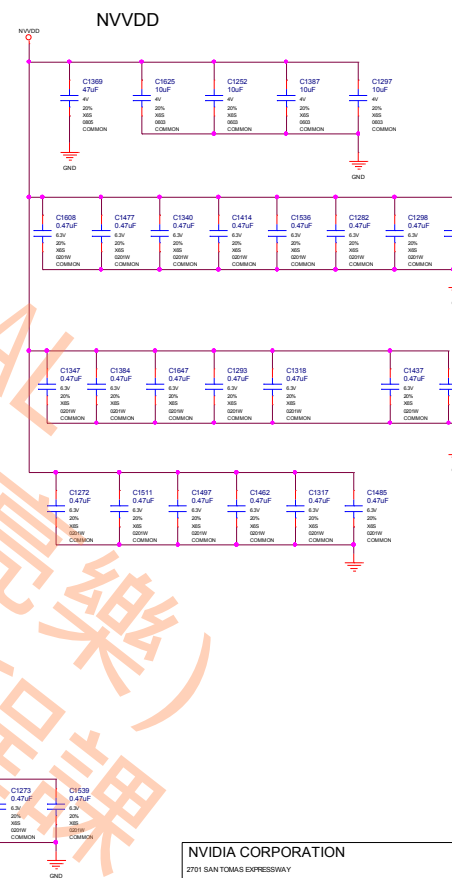
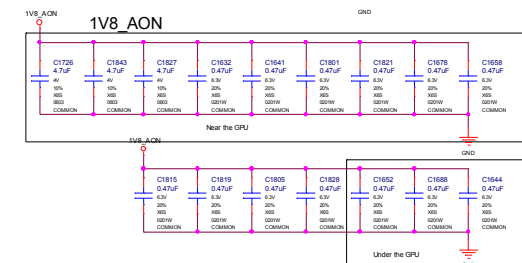
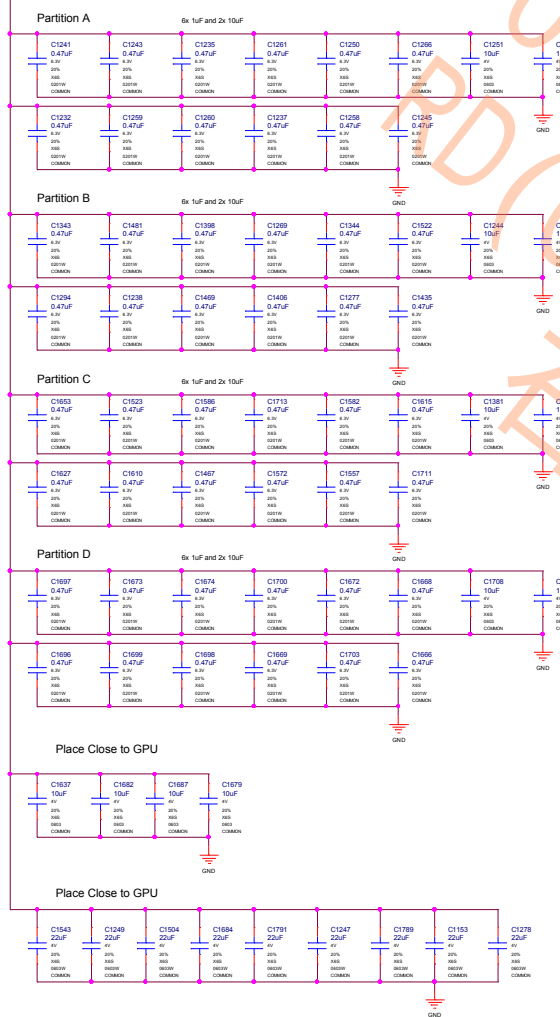




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NVVDD

FBVDDQ



032-0532-000

XBS
0805

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PAGE DETAIL	GPU Decoupling

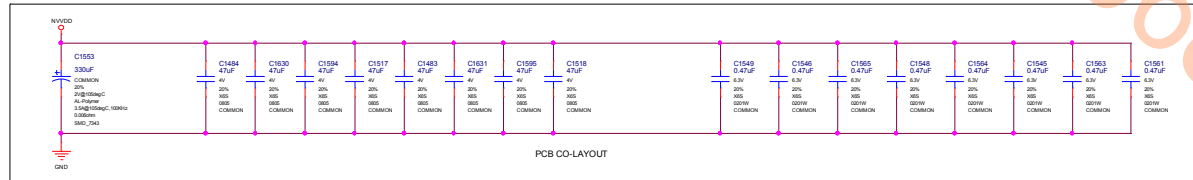
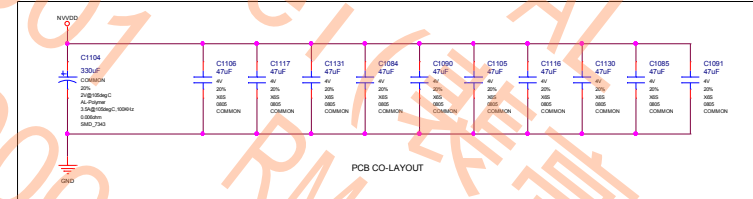
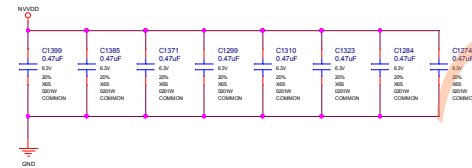
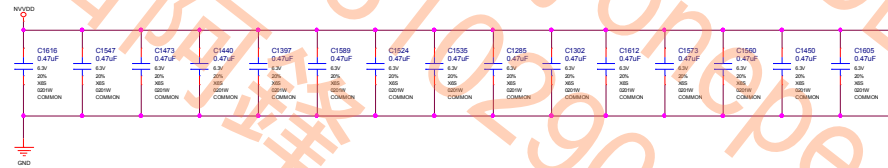
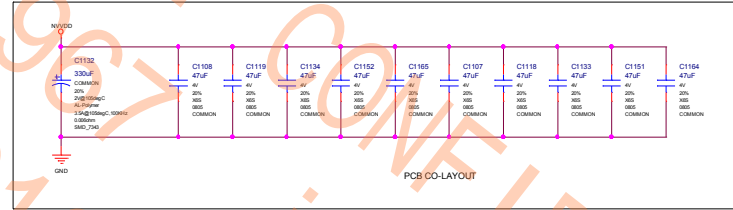
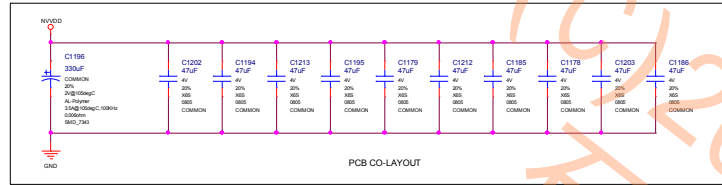
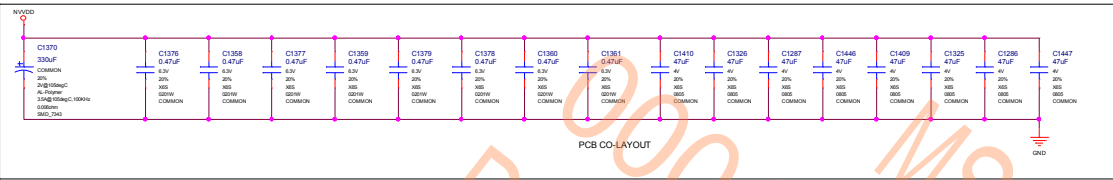
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PCB DETAIL	GPU DECOUPLING

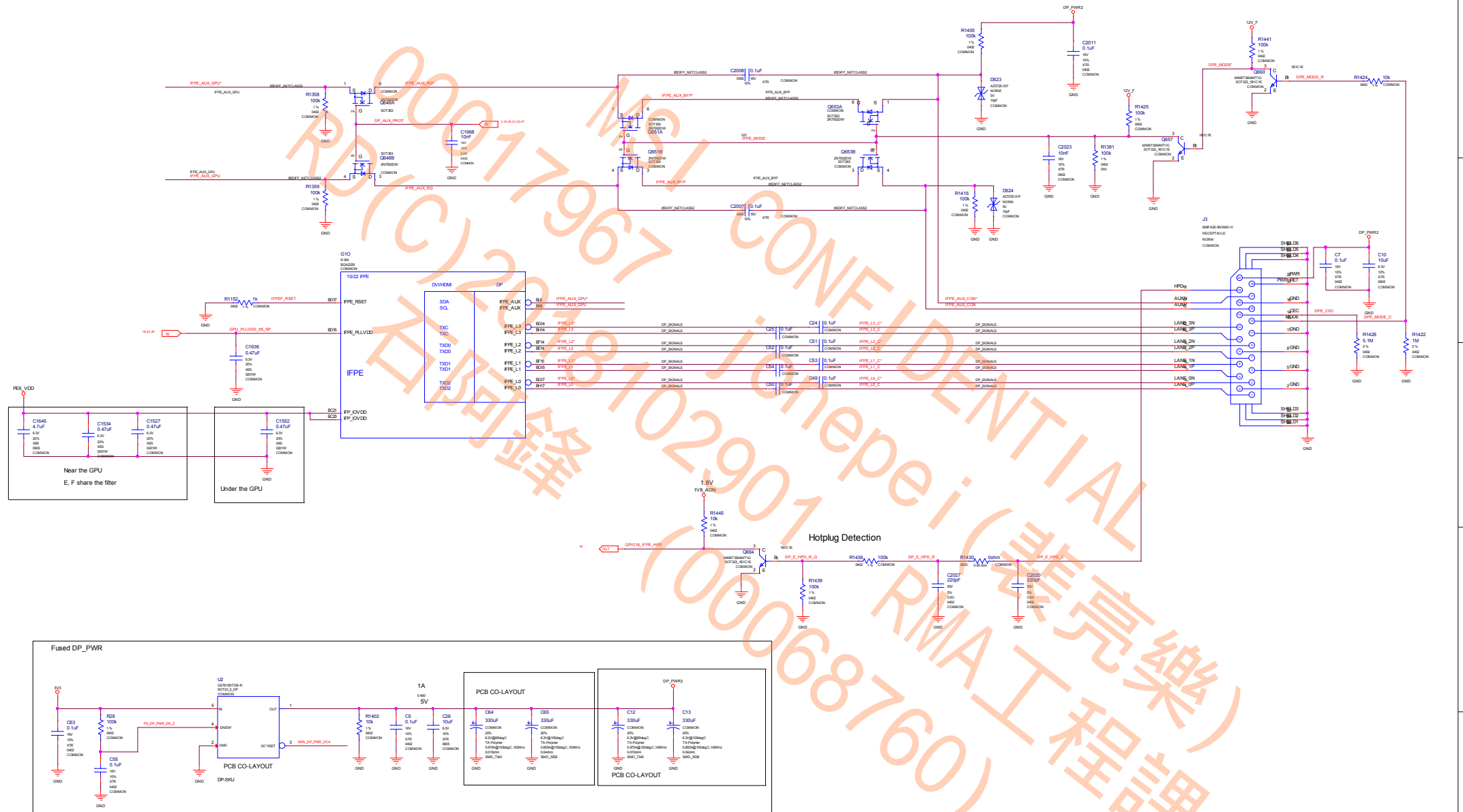
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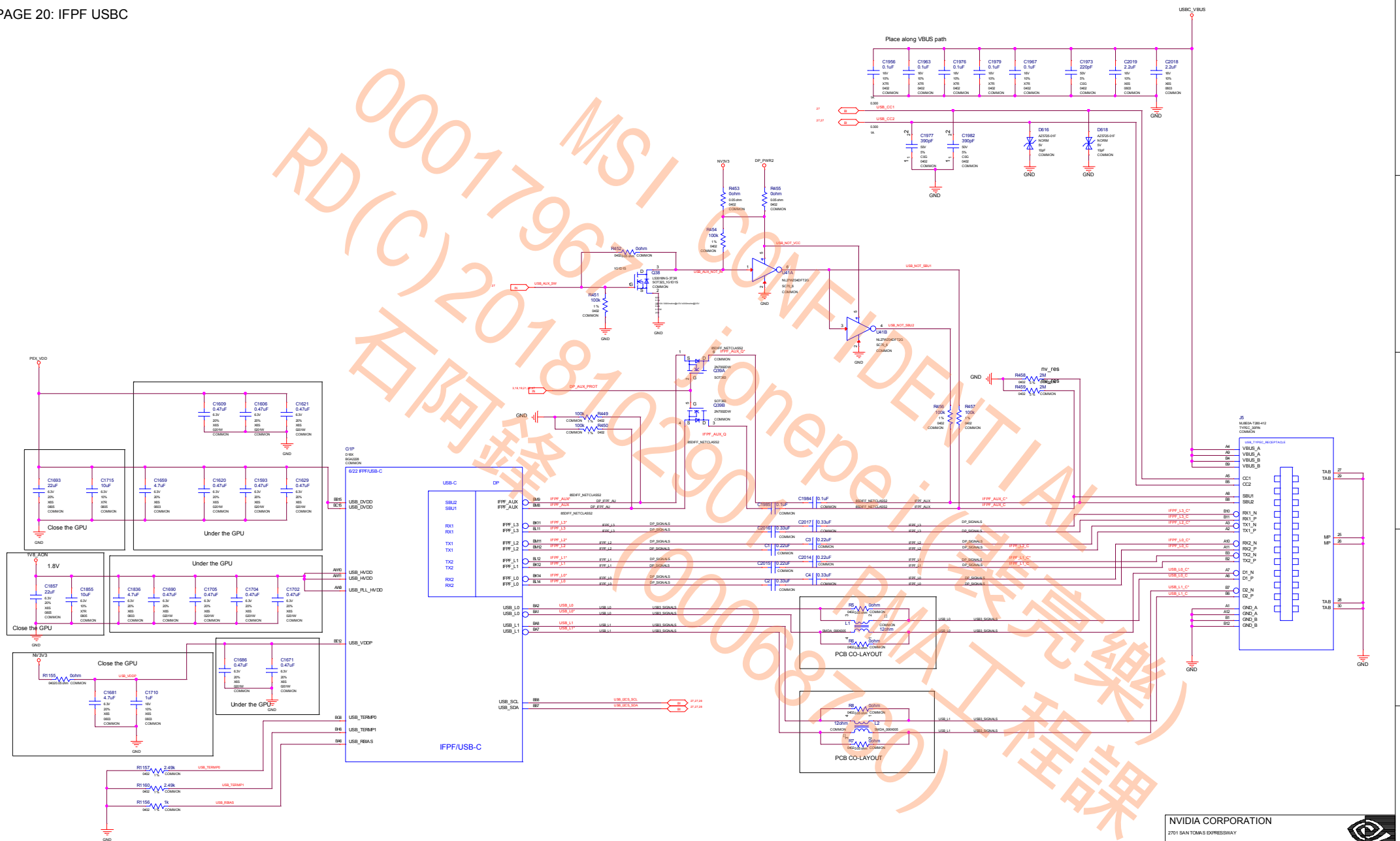
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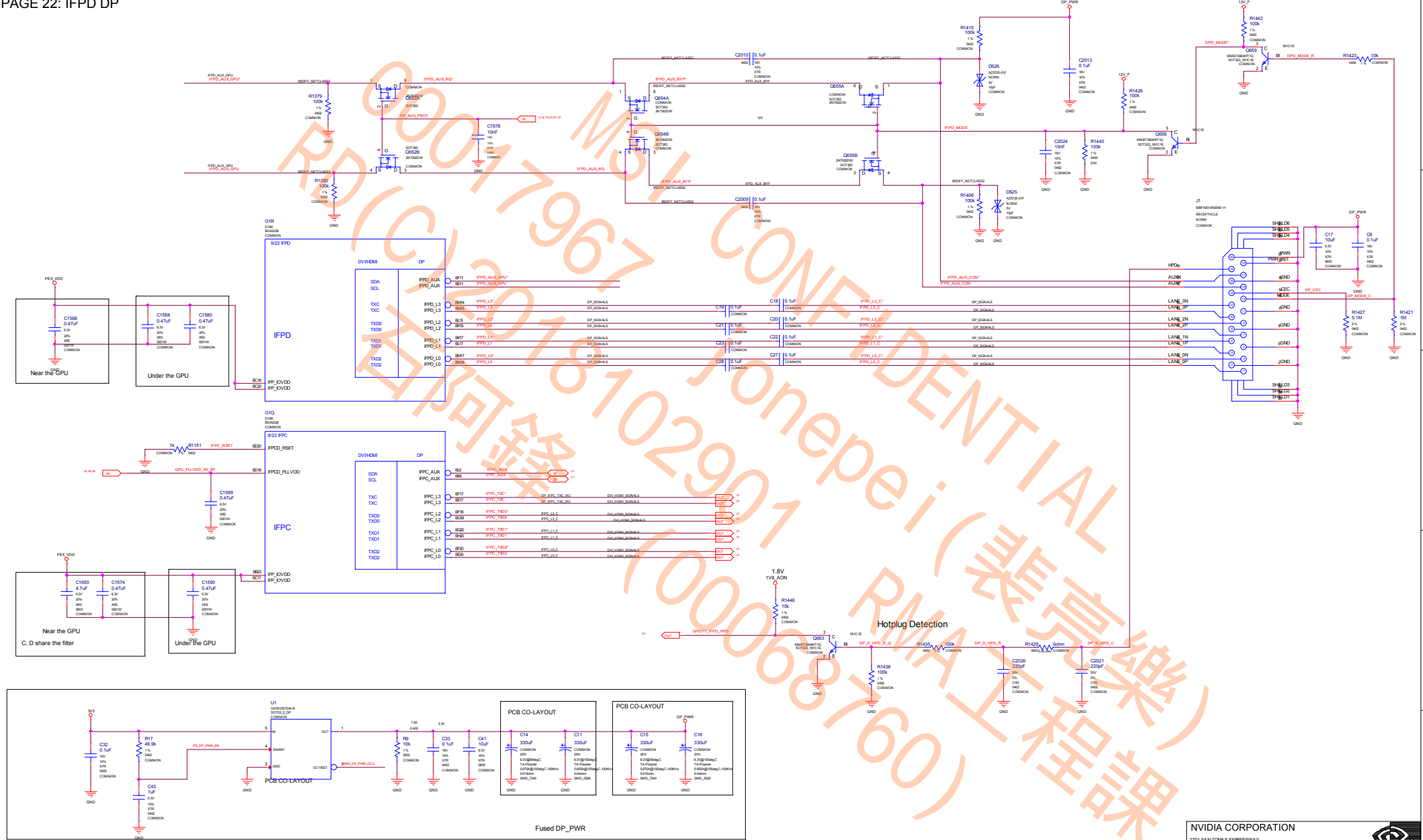


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H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

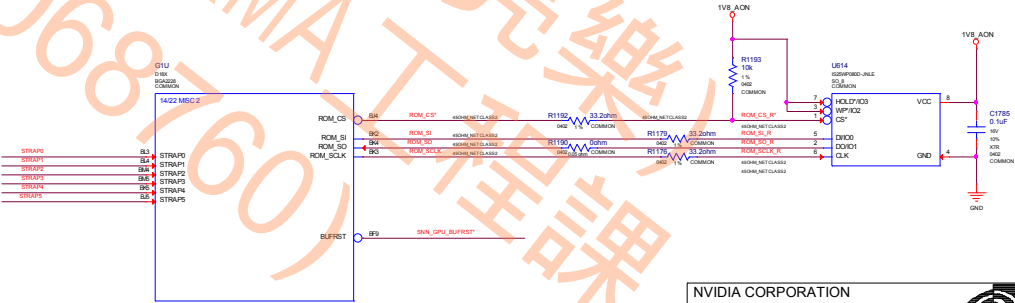
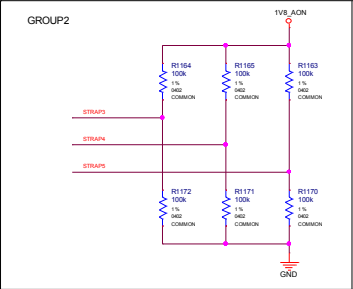
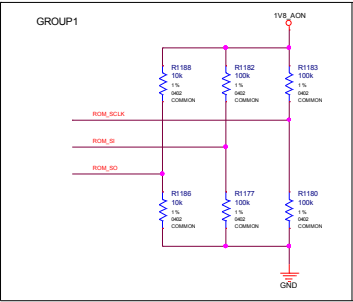
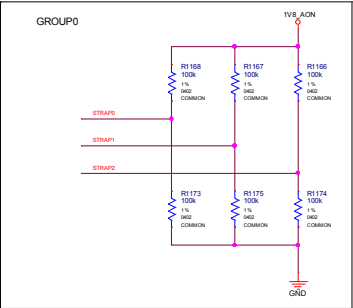
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]	FS_OVERT	
L	L	L	XXX1	1:ENABLE 0:DISABLE	
L	L	M	XXX0	FS_OVERT ENABLE	
L	L	M	XXX0	FS_OVERT DISABLE	

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	1
M	H	L	1	1	1	1	0
M	L	H	1	1	0	1	1
M	L	L	1	1	0	0	0
L	H	M	1	0	1	1	1
L	M	H	1	0	1	0	0
L	M	L	1	0	0	1	1
L	L	M	1	0	0	0	0
H	H	H	0	1	1	1	1
H	H	L	0	1	1	0	0
H	L	H	0	1	0	1	1
H	L	L	0	1	0	0	0
L	H	H	0	0	1	1	1
L	H	L	0	0	1	0	0
L	L	H	0	0	0	1	1
L	L	L	0	0	0	0	0

Default

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung



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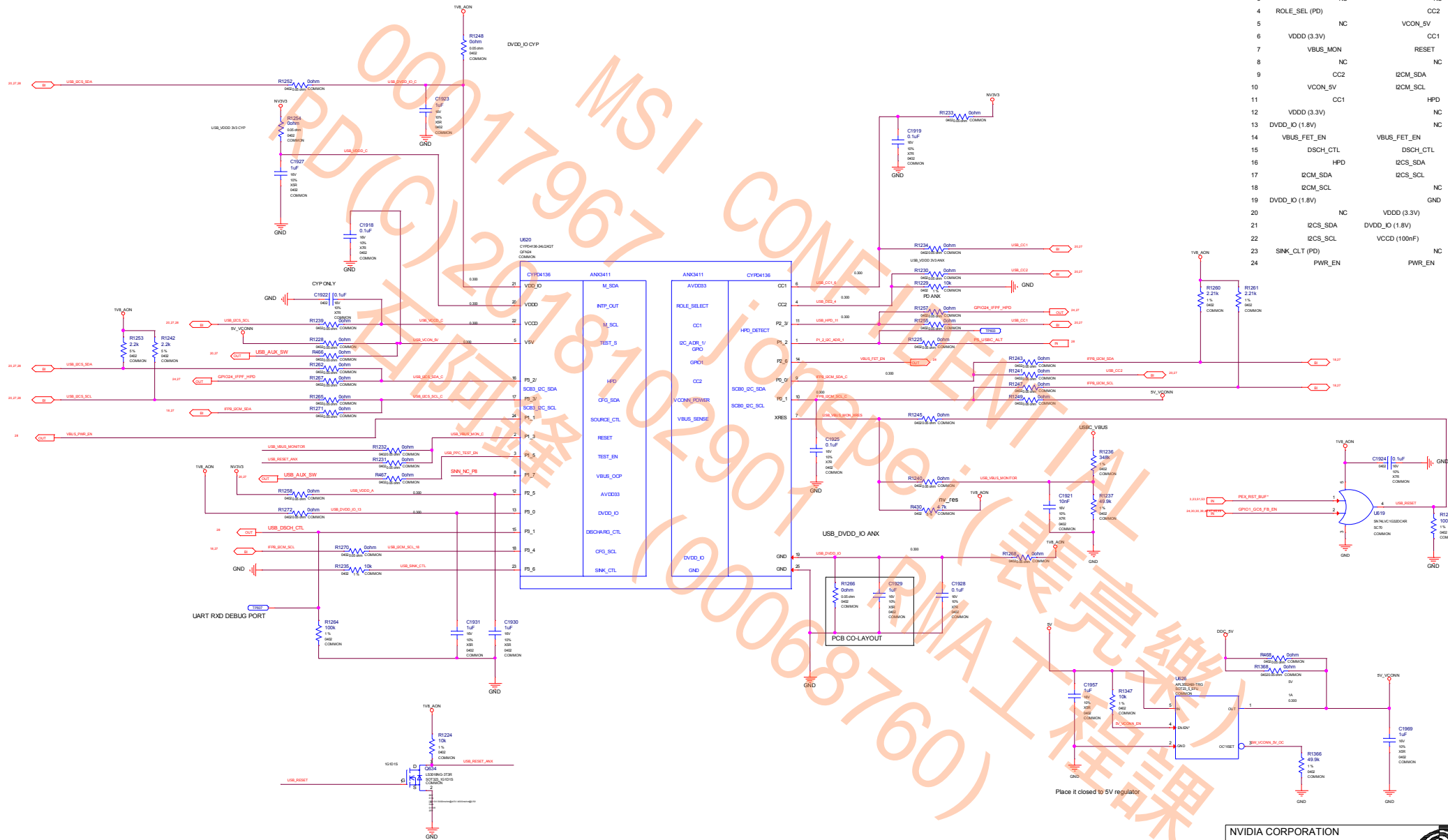
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PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_SV
6	VDDO (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_SV	I2CM_SCL
11	CC1	HPD
12	VDDO (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDO (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100nF)
23	SINK_CTL (PD)	NC
24	PWR_EN	PWR_EN

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC USB PPC

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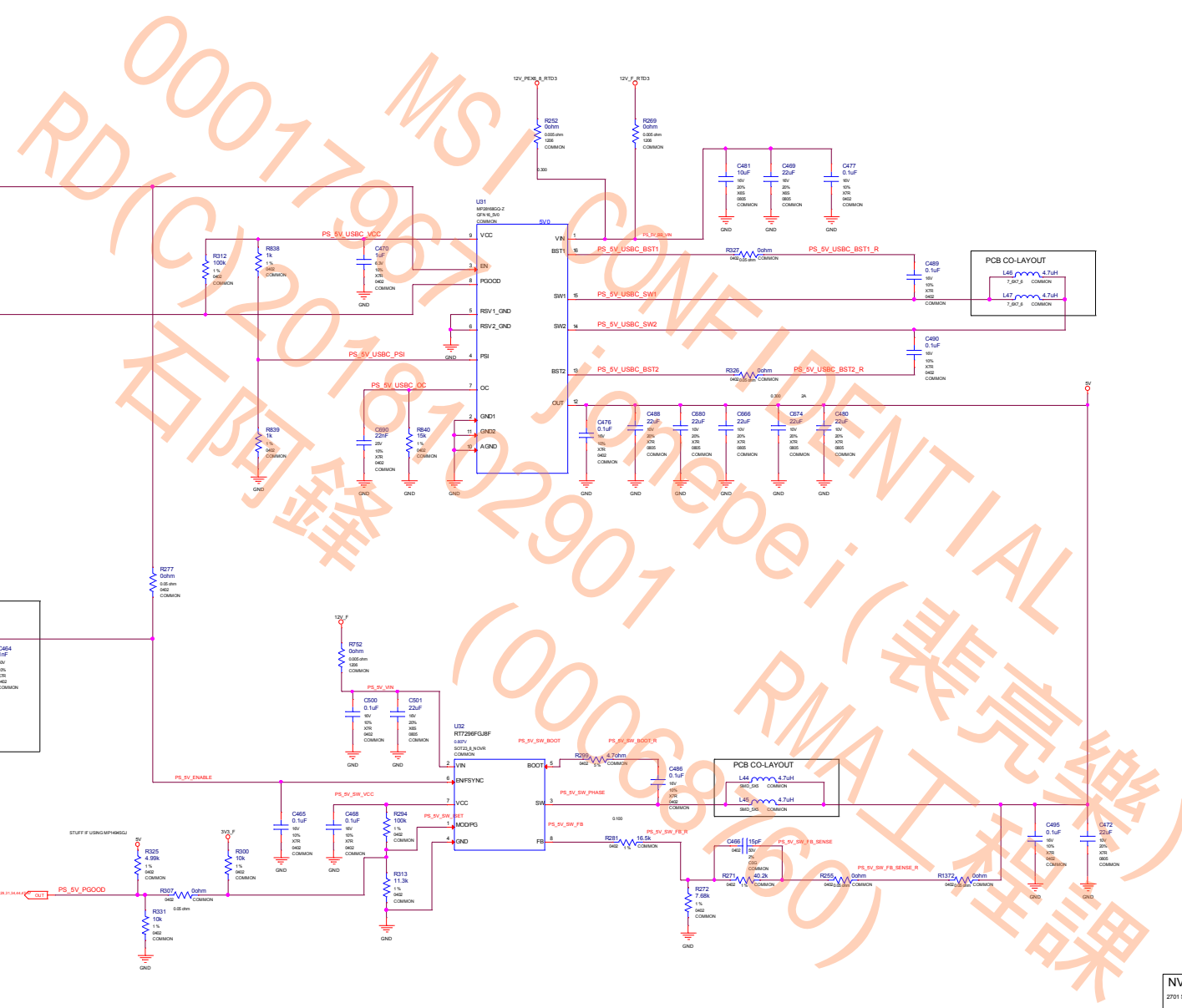
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PAGE DETAIL	PS: 5V, 5V BACKUP

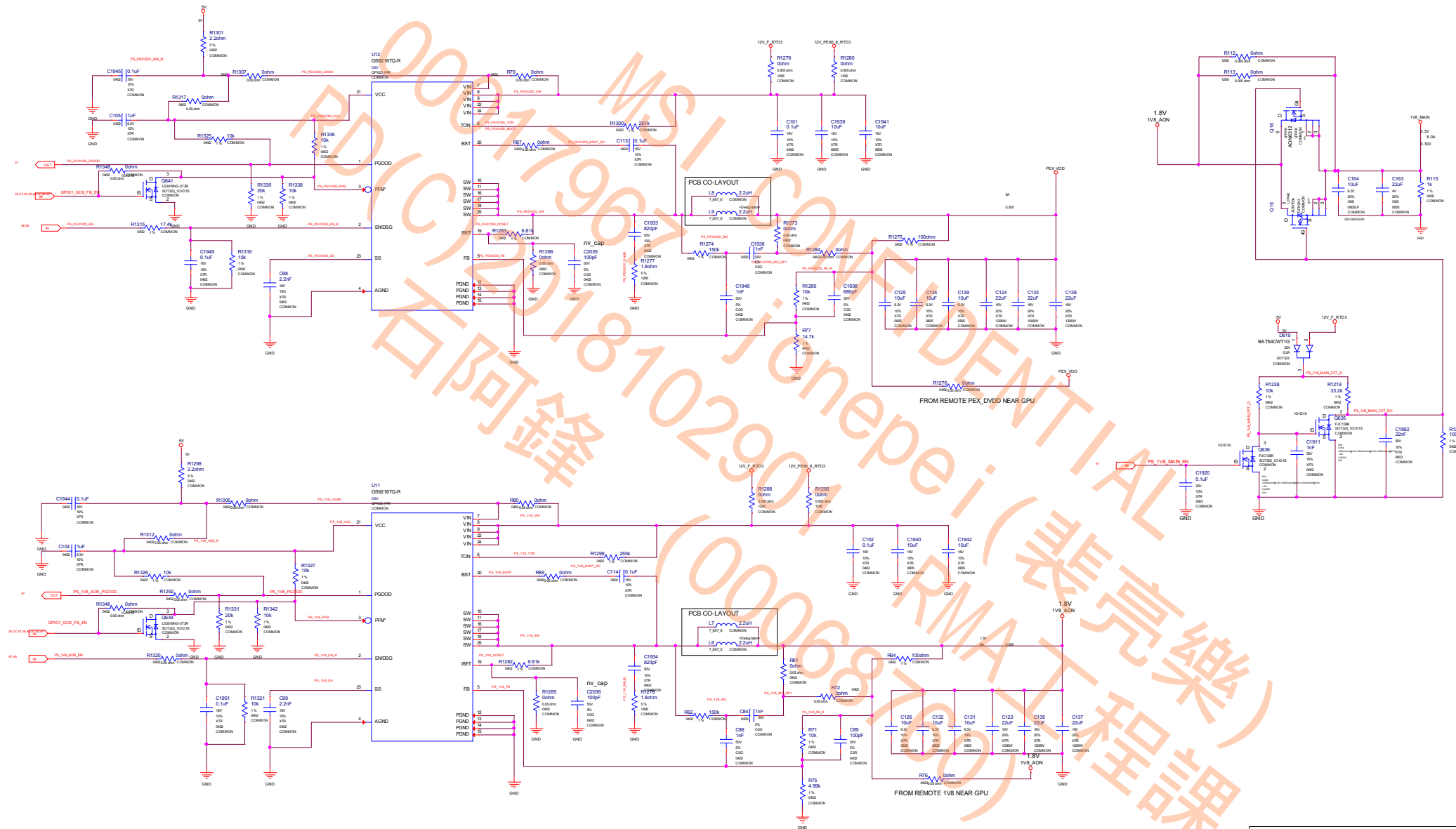
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: PEXVDD, 1V8

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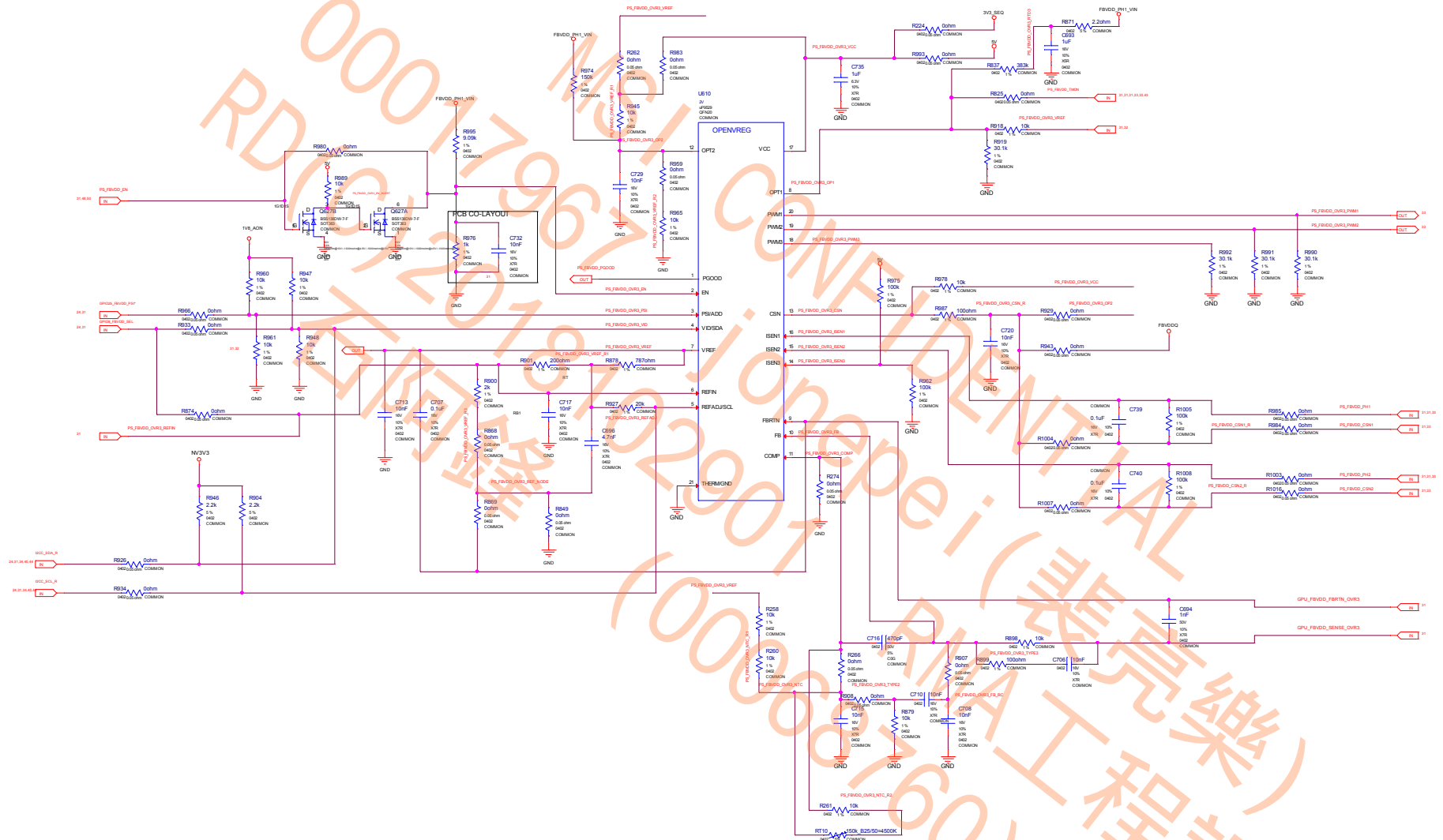
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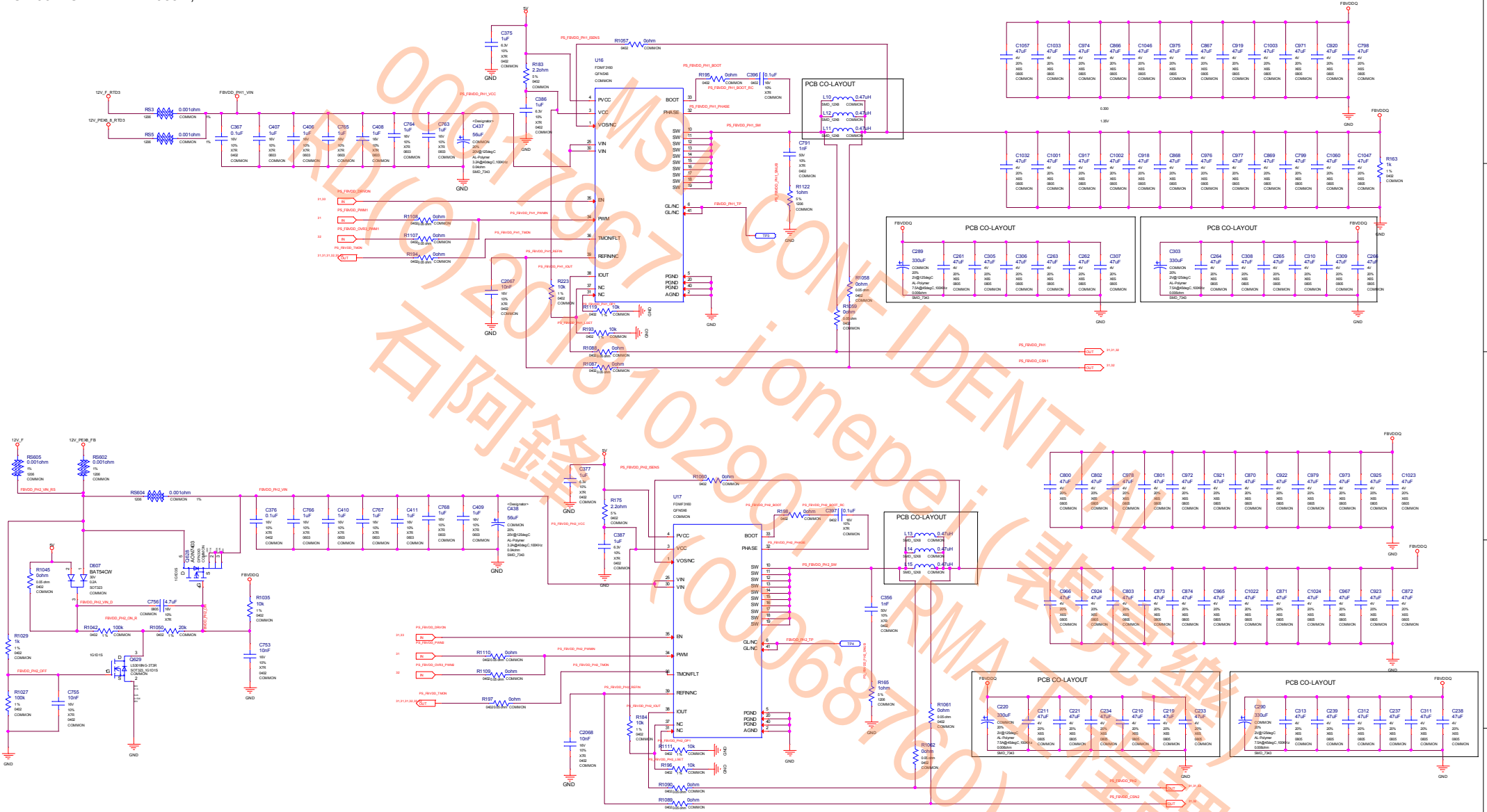
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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	PS: FBVDD PHASE 1, 2

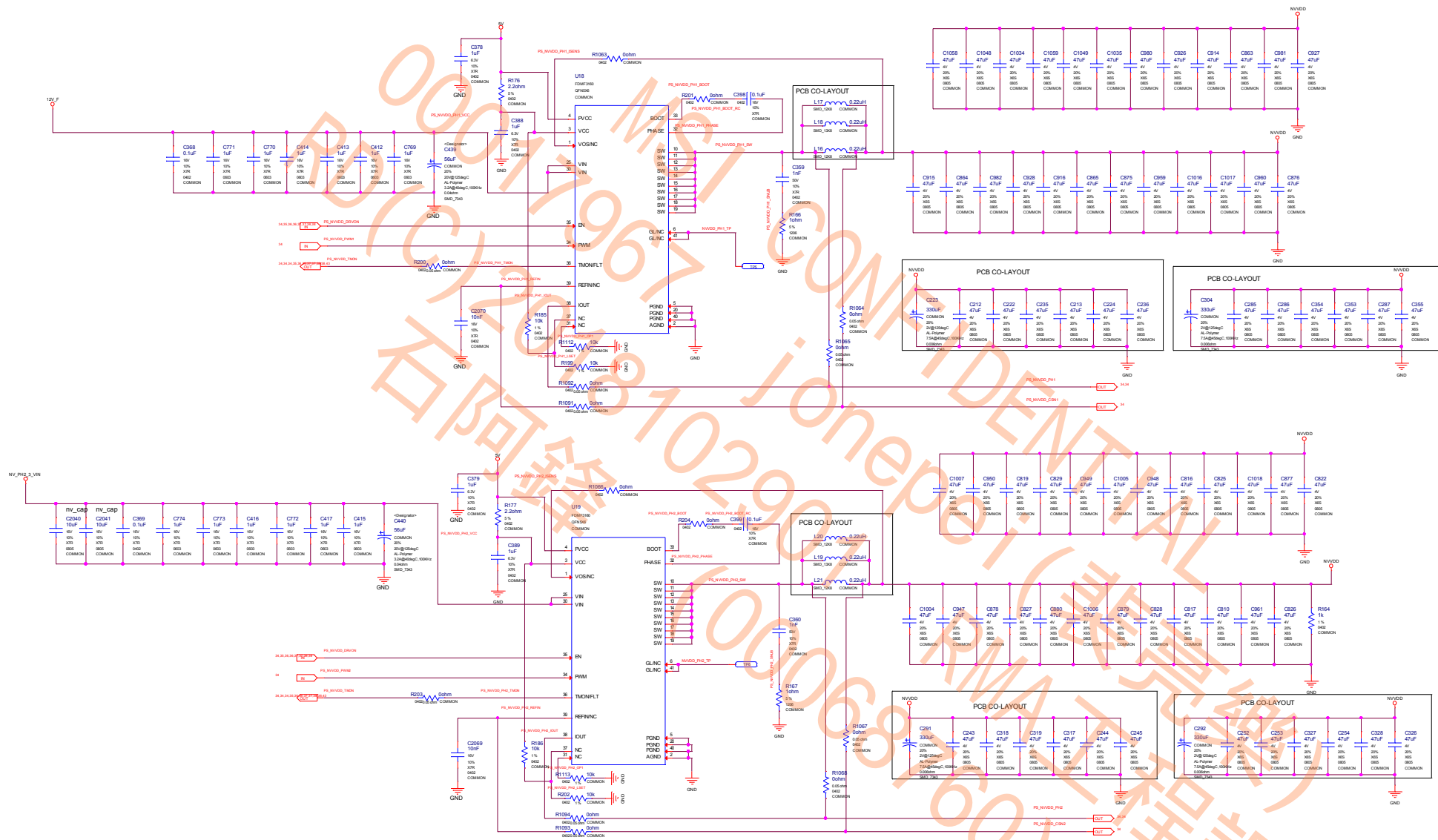
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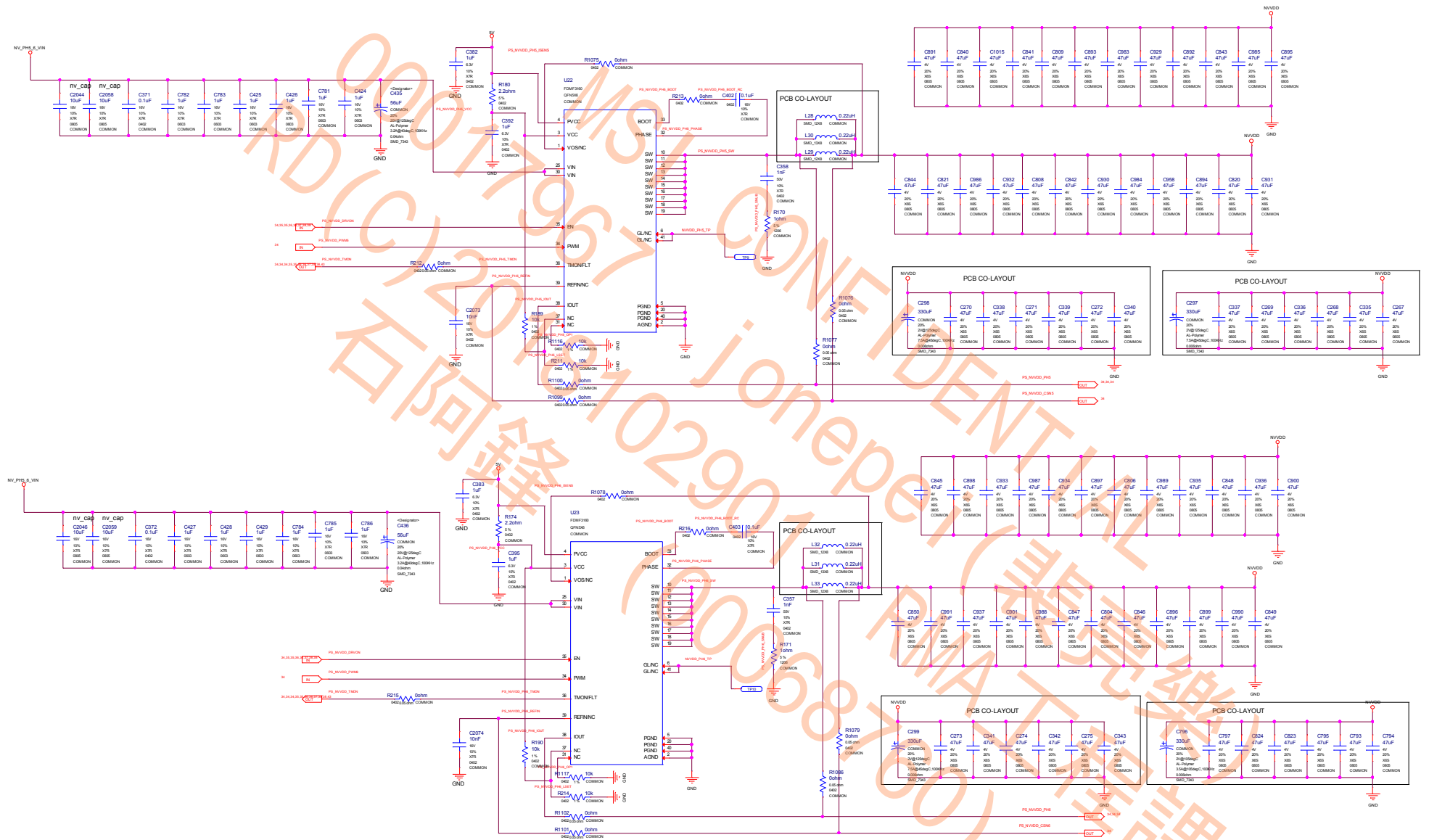


ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	PS: NVVDD Phase 1, 2

600-1G180-BASE-200

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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	PS: NVVDD Phase 5, 6

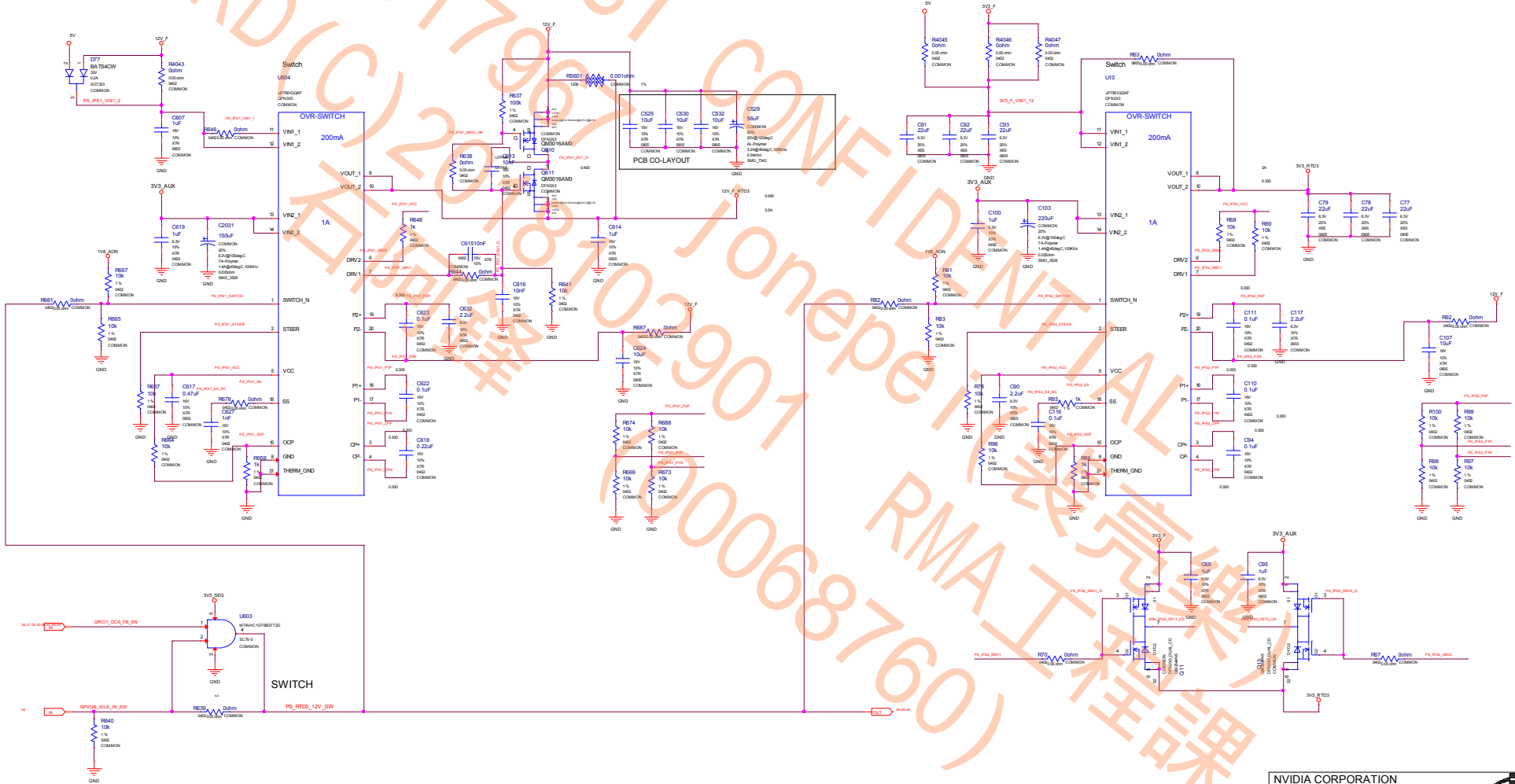
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AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A



ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE: 39	PS: INPUT SWITCH RTD3

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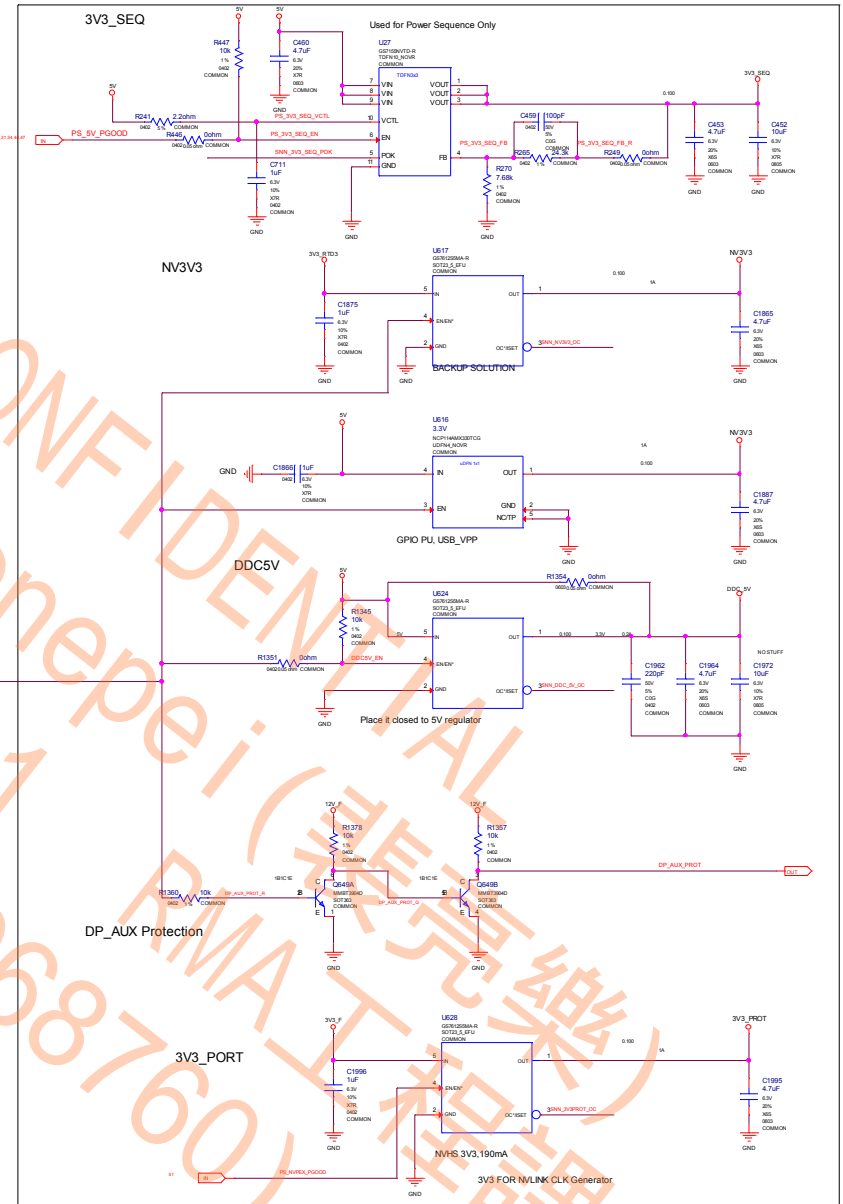
NV_PN 600-1G180-BASE-200

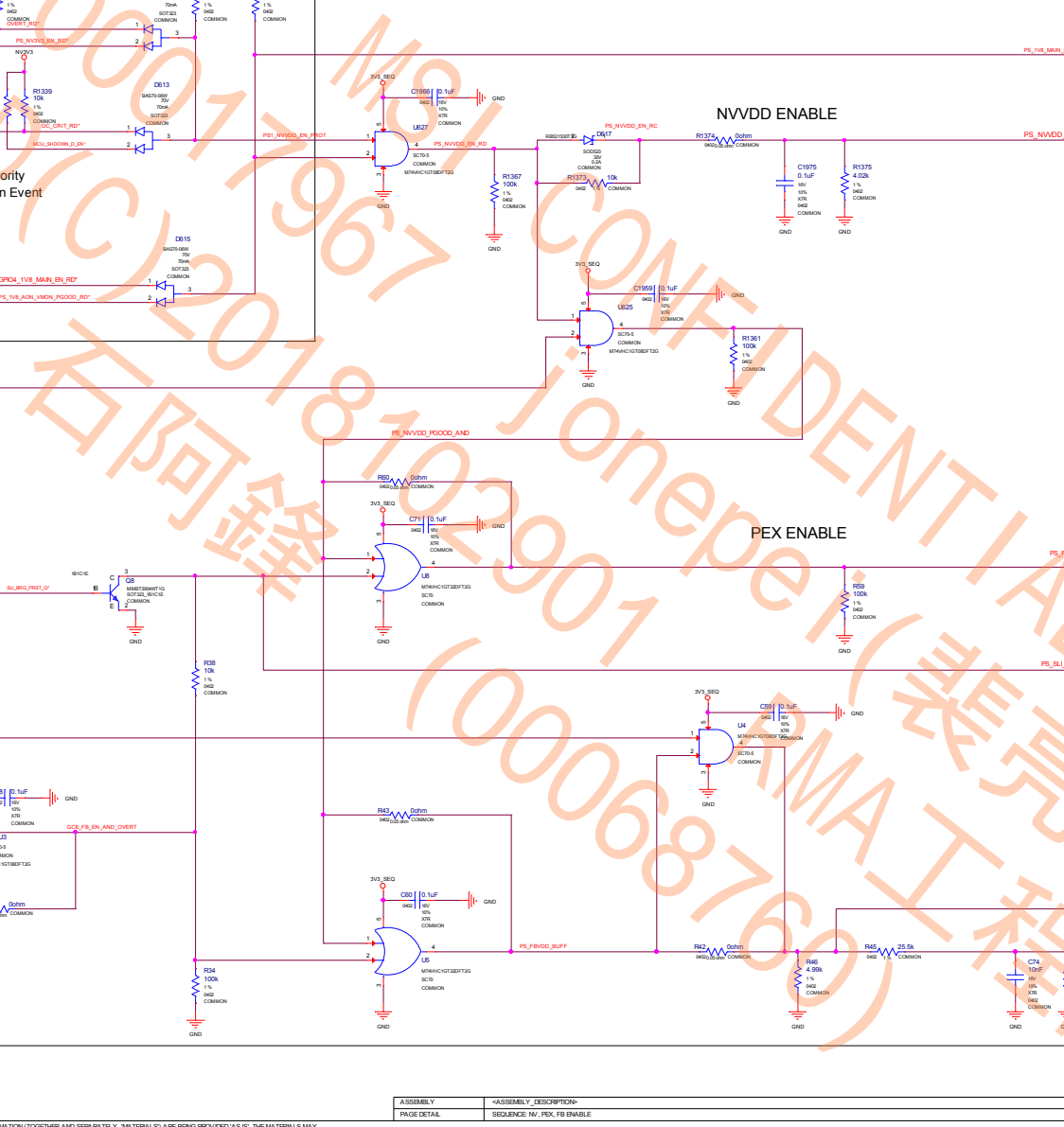
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Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIe golden finger
12V	INPUT	Sense the 12V Voltage from PCIe golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating[1]h once both 3V3 and 12V reach Vth
G06_FB_EN	INPUT	Indicator for RTD3/G06 residence.Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSK	INPUT	From INA3221(PV) or Pre-filter(BS_K)
PS_RTD3_12V_SW	INPUT	G06_FB_EN && ILE_IN_SW



OPTIONS	PEX0V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Pre_Filter(ADC_MUX):3V3(PEX)

Only use the Primary Pre-Filter to sense 3V3PEX
and All Input 12Vs

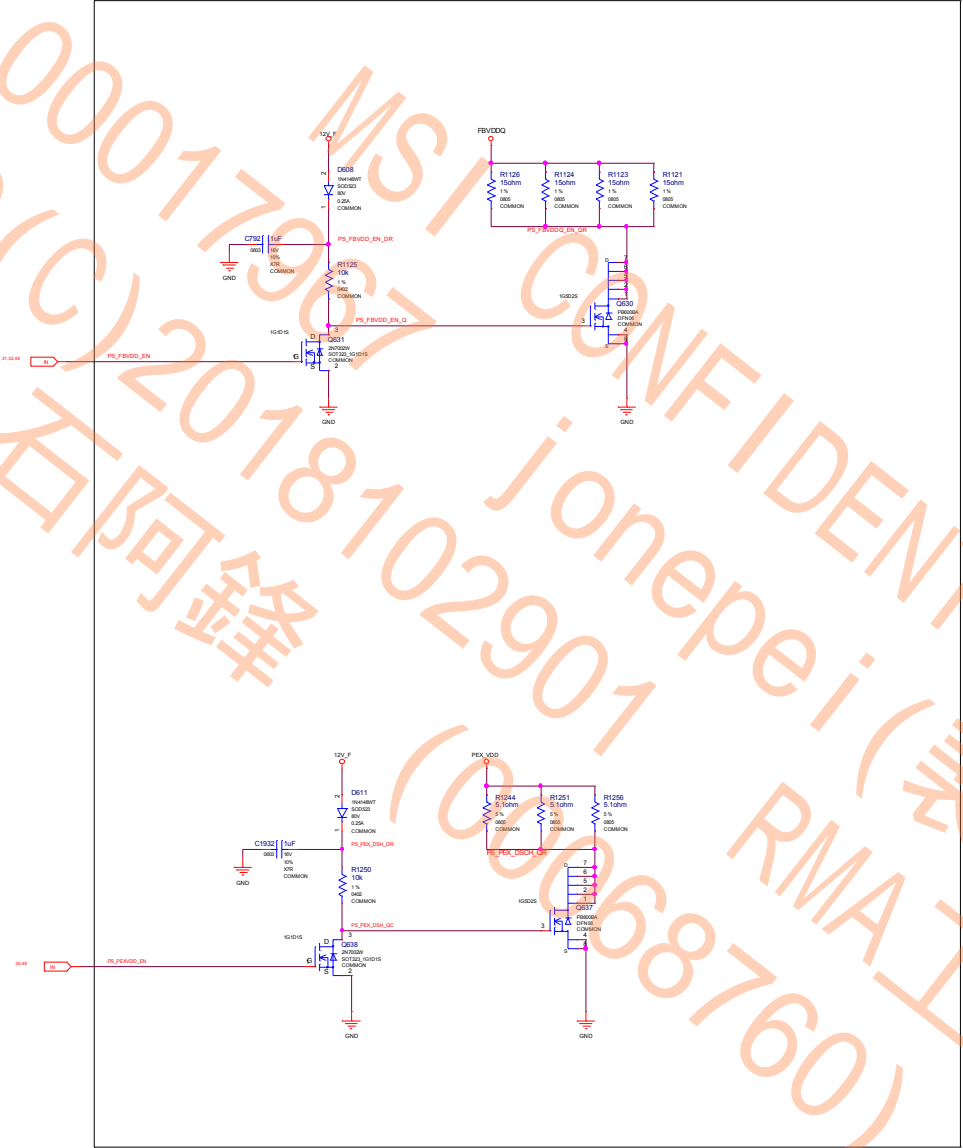
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PAGE DETAIL	SEQUENCE: POE VOLTAGE MONITOR

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PCB REV	PG180-A02
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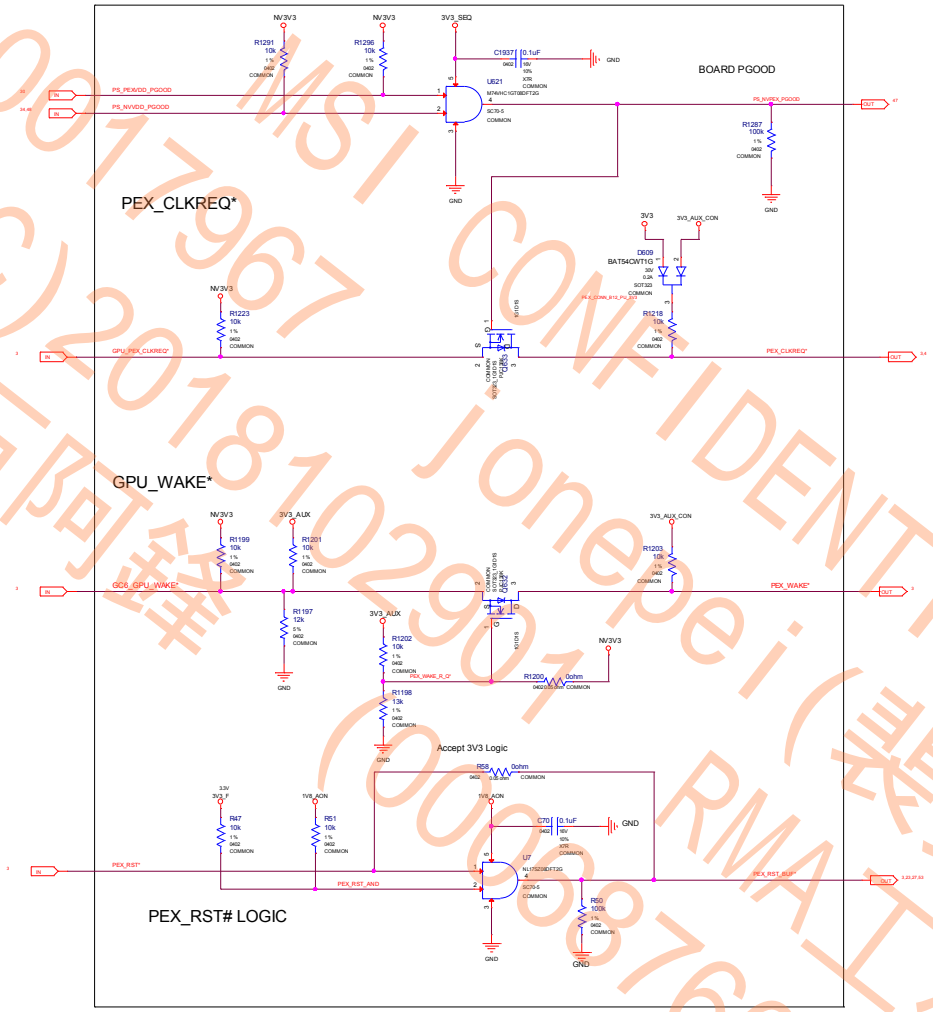
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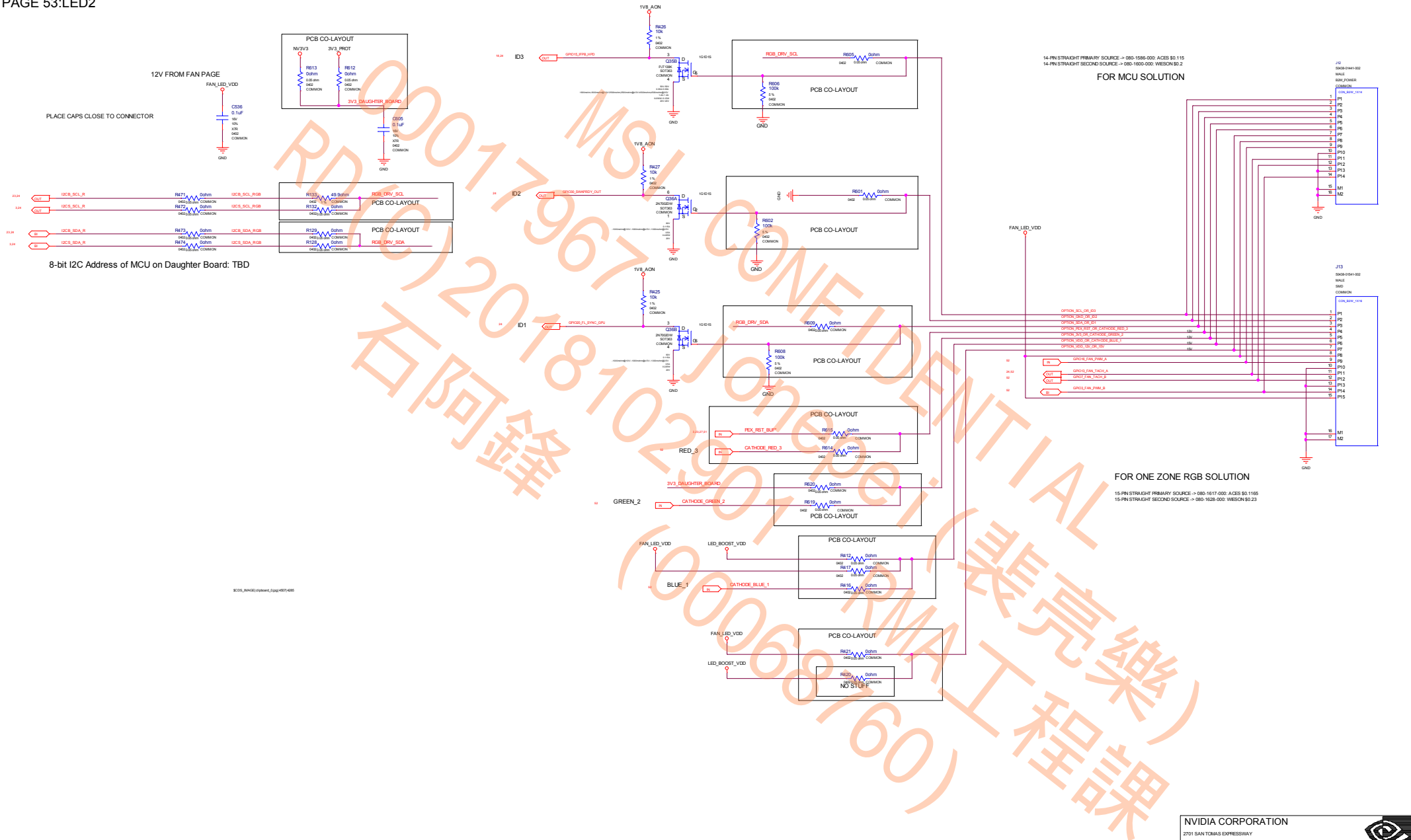
ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	SEQUENCE: DISCHARGE

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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	LED 2

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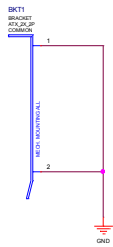
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Brackets:



Bracket Screw



BOARD STIFFENER



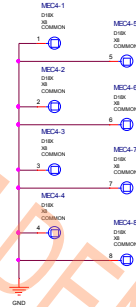
STIFFENER

GPU Socket Symbol

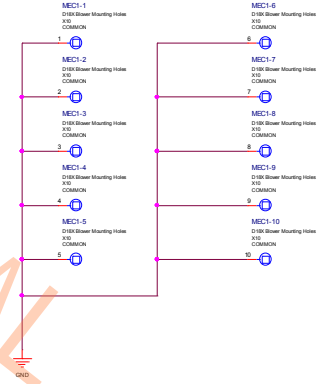
BGA SOCKET ASSY



GPU Mounting holes



Mechanical Holes Symbol



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